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CmpE 124 Lab 6:Greater-Than Design

Anahit Sarao, 008435583, CmpE 124 Spring 2015, Lab Section 2

*Abstract*—This labs purpose was to create a 2 bit unsigned and 4 bit signed comparator using logic gates and Boolean Equations. The greater-than and equal-to comparators were designed and tested using 2 bit unsigned and 4 bit signed bits.

# INTRODUCTION

In this lab two comparators were designed and tested. By creating truth tables and kmaps the equations were found then the voltage table was used to test the design. For the two bit unsigned numbers the bits were compared for greater than values. For the 4 bit signed a greater-than and equal comparator was designed. The design and testing was done in logicworks software.

# Design methodology

## Parts List

* Logicworks

## Truth Tables

2-bit Unsigned Greater-Than Comparator Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| b | | a | | F |
| b1 | b0 | a1 | a0 | F(a>b) |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

4-bit Signed Equal-To Comparator Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comparing Inputs | | | | Output |
| a3b3 | a2 b2 | a1b1 | a0b0 | F(a=b) |
| a3> b3 | X | X | X | 0 |
| a3<  b3 | X | X | X | 0 |
| a3=  b3 | a2>  b2 | X | X | 0 |
| a3=  b3 | a2  < b2 | X | X | 0 |
| a3=  b3 | a2 = b2 | a1> b1 | X | 0 |
| a3=  b3 | a2 = b2 | a1< b1 | X | 0 |
| a3=  b3 | a2 = b2 | a1= b1 | a0> b0 | 0 |
| a3=  b3 | a2 = b2 | a1= b1 | a0< b0 | 0 |
| a3=  b3 | a2 = b2 | a1= b1 | a0= b0 | 1 |

4-bit Signed Greater-Than Comparator Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comparing Inputs | | | | Output |
| a3b3 | a2 b2 | a1b1 | a0b0 | F(a>b) |
| a3> b3 | X | X | X | 1 |
| a3<  b3 | X | X | X | 0 |
| a3=  b3 | a2>  b2 | X | X | 1 |
| a3=  b3 | a2  < b2 | X | X | 0 |
| a3=  b3 | a2 = b2 | a1> b1 | X | 1 |
| a3=  b3 | a2 = b2 | a1< b1 | X | 0 |
| a3=  b3 | a2 = b2 | a1= b1 | a0> b0 | 1 |
| a3=  b3 | a2 = b2 | a1= b1 | a0< b0 | 0 |
| a3=  b3 | a2 = b2 | a1= b1 | a0= b0 | 0 |

2-bit Unsigned Greater-Than Comparator Voltage Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| b | | a | | F |
| b1 | b0 | a1 | a0 | F(a>b) |
| L | L | L | L | L |
| L | L | L | H | H |
| L | L | H | L | H |
| L | L | H | H | H |
| L | H | L | L | L |
| L | H | L | H | L |
| L | H | H | L | H |
| L | H | H | H | H |
| H | L | L | L | L |
| H | L | L | H | L |
| H | L | H | L | L |
| H | L | H | H | H |
| H | H | L | L | L |
| H | H | L | H | L |
| H | H | H | L | L |
| H | H | H | H | L |

4-bit Signed Equal-To Comparator Voltage Table

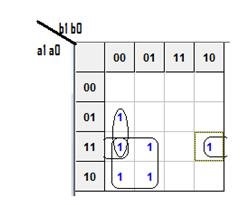
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comparing Inputs | | | | Output |
| a3b3 | a2 b2 | a1b1 | a0b0 | F(a=b) |
| a3> b3 | X | X | X | L |
| a3<  b3 | X | X | X | L |
| a3=  b3 | a2>  b2 | X | X | L |
| a3=  b3 | a2  < b2 | X | X | L |
| a3=  b3 | a2 = b2 | a1> b1 | X | L |
| a3=  b3 | a2 = b2 | a1< b1 | X | L |
| a3=  b3 | a2 = b2 | a1= b1 | a0> b0 | L |
| a3=  b3 | a2 = b2 | a1= b1 | a0< b0 | L |
| a3=  b3 | a2 = b2 | a1= b1 | a0= b0 | H |

4-bit Signed Greater-Than Comparator Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comparing Inputs | | | | Output |
| a3b3 | a2 b2 | a1b1 | a0b0 | F(a>b) |
| a3> b3 | X | X | X | L |
| a3<  b3 | X | X | X | H |
| a3=  b3 | a2>  b2 | X | X | H |
| a3=  b3 | a2  < b2 | X | X | L |
| a3=  b3 | a2 = b2 | a1> b1 | X | H |
| a3=  b3 | a2 = b2 | a1< b1 | X | L |
| a3=  b3 | a2 = b2 | a1= b1 | a0> b0 | H |
| a3=  b3 | a2 = b2 | a1= b1 | a0< b0 | L |
| a3=  b3 | a2 = b2 | a1= b1 | a0= b0 | L |

## Karnaugh Maps

F(a>b) = a1 b1` + b1` b0` a0 + a1 a0 b0`



## Original and Derived Equations

2-bit Unsigned Greater-Than Comparator

F(a>b) = a1 b1` + b1` b0` a0 + a1 a0 b0`

4-bit Signed Equal-To Comparator

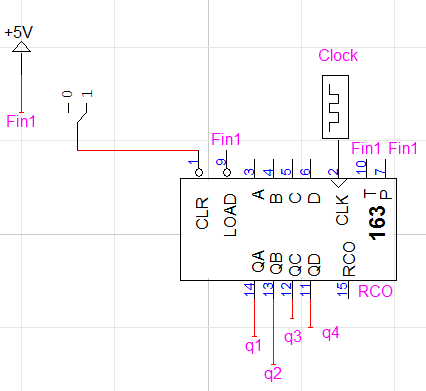
F(a=b) = (a3 ʘ b3)  (a2 ʘ b2)  (a1 ʘ b1) (a0ʘ  b0)

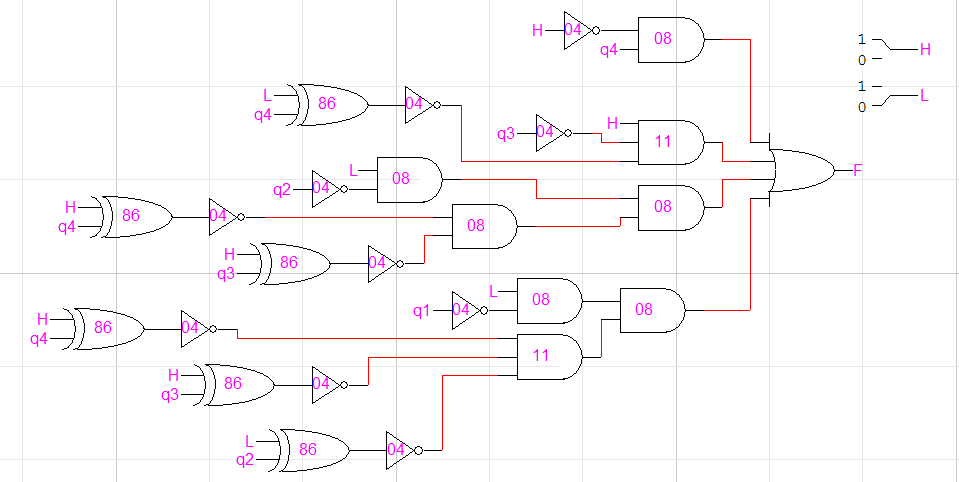
4-bit Signed Greater-Than Comparator

F(a>b) = a1 b1` + (a3 ʘ b3)  (a2 ʘ b2)  (a1 ʘ b1)  a0 b0`

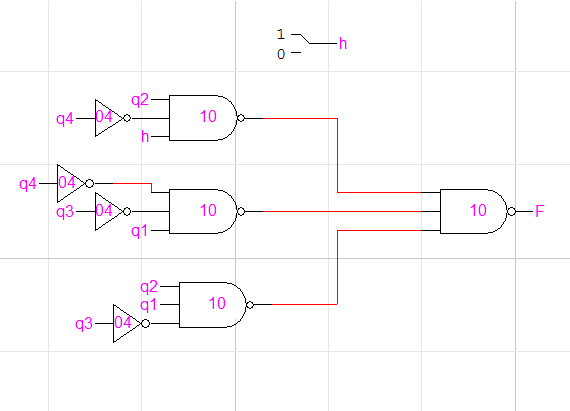
## Schematics

Schematic 1: Clock and Signal Inputs

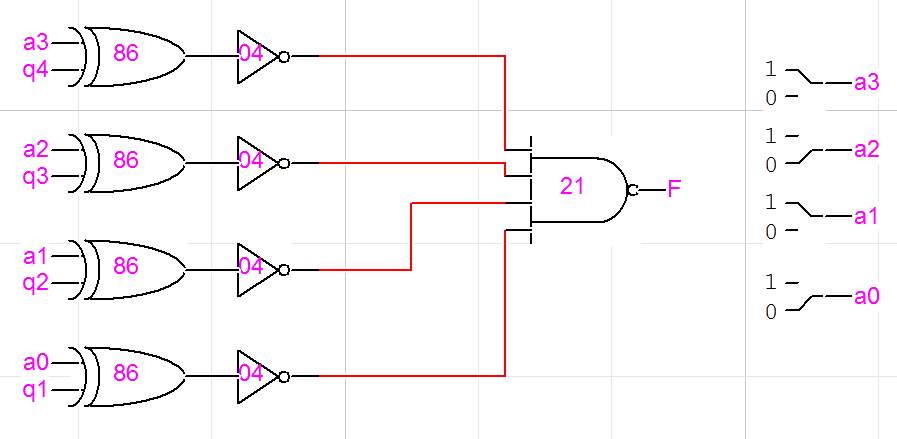




Schematic 2: 2-bit Unsigned Greater-Than Comparator



Schematic 3: 4-bit Signed Equal-To Comparator

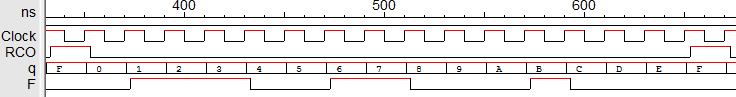


Schematic 4: 4-bit Signed Greater-Than Comparator

# testing procedures

The testing procedure should be broken down into steps:

1. Create a KMAP for each comparator, and then reduce the equation to the simplest form.
2. Make a truth and voltage table that satisfies the equation.
3. Design and create the logical circuit in logicworks.
4. Test the circuit using the truth table to see if the logical circuit is designed properly.

Figure 1: 2-bit Unsigned Greater-Than Comparator

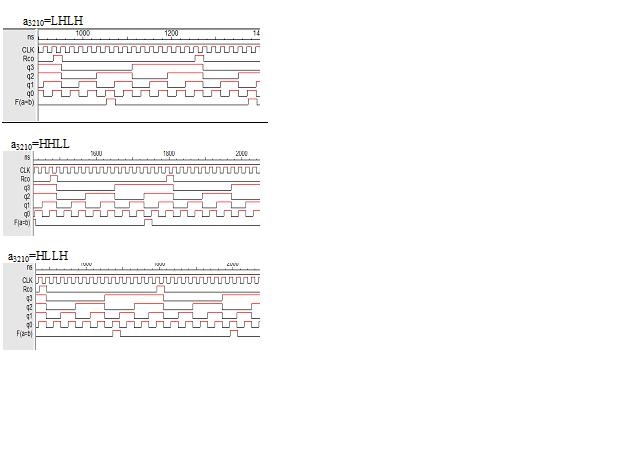
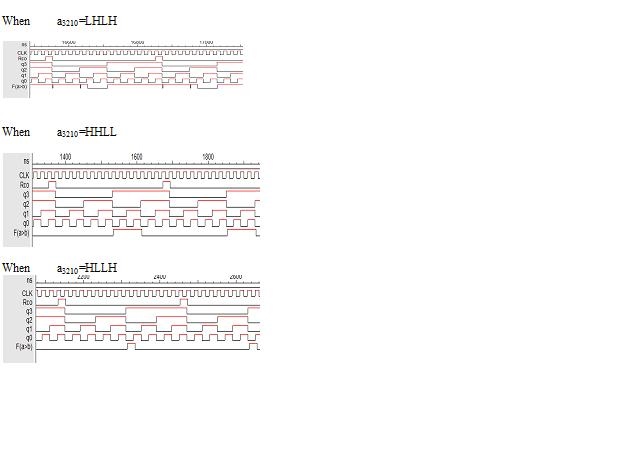
Figure 2: 4-bit Signed Equal-To Comparator

Figure 3: 4-bit Signed Greater-Than Comparator



# testing results

For the 2-bit unsigned bit greater than comparator the output would be high if the bit B was greater than bit A. Looking at figure 1 we can see that F the output is high during the clock count of 1-3, 6-7, and 11. This is confirmed by the truth table. For the equal-to comparator the A bit was manually controlled to try 3 different combinations. For each test the output was true only one during a single period of the clock. Output was triggered when the 4 bit signed number matched the clocks count.

Figure 2 shows three different tests of the circuit. The 4-bit signed greater –than comparator was the same design as the 2 bit unsigned but instead 2 more bits where used. The adding of the two bits added more gates hence certain tests yielded glitches shown in figure 4.

# Conclusion

This lab helped understand how digital logic can be used to build circuits that can perform functions of great use. In this lab 3 different comparators were designed a 2-bit unsigned great-than and a 4-bit signed greater than or equal to. The 2 bit comparator simply compares each bit and shows the result. While the 4-bit initially checks the MSB then decides if the next bit is needed to be compared or to stop.

# appendices and references

N/A

1. Anahit Sarao, indianvip60@gmail.com [↑](#footnote-ref-1)